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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,836	02/25/2002	Masahiko Yukawa	09792909-5346	1041

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SONNENSCHEIN NATH & ROSENTHAL LLP
P.O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606-1080

EXAMINER	
DANIELS, ANTHONY J	

ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
12/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/082,836	YUKAWA ET AL.	
	Examiner	Art Unit	
	Anthony J. Daniels	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,18 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/16/2007 has been entered.

Response to Arguments

1. Applicant's arguments with respect to the independent claims and the Watanbe reference have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1,5,9,18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanbe et al. (Japanese Publication Number: H09-055487) in view of Shinbori et al. (US # 4,594,613).

As to claim **1**, Watanbe et al. teaches a solid-state image pickup device (see Watanbe et al., Drawings 1,2 and 3) comprising: a circuit board (see Watanbe et al., Drawings 2 and 3, circuit board "22") having a first opening (see Watanbe et al., Drawing 2, opening aperture "23"); a sensor package with a second opening (see Watanbe et al., Drawing 2 and 3, solid-state image sensor package "20"; [0016], Lines 1-6) in which a chip of a solid-state image pickup element with a light-receiving surface is placed (see Watanbe et al., Drawing 2 and 3, sensor chip "11"; Drawing 1, light-receiving side "12"), the sensor package disposed at one surface of the circuit board so that the light-receiving surface of the chip of the solid-state image pickup element opposes said first opening of the circuit board (see Watanbe et al., Drawing 3); a seal adhered to the sensor package for sealing in the solid-state image pickup element (see Watanbe et al., Drawings 2 and 3, transparence plate "19" in opening "23" of circuit board "22"); and an optical unit disposed at the other surface of the circuit board so that incident light is focused on the light-receiving surface (see Watanbe et al., Drawings 2 and 3, lens unit "25"); wherein the circuit board is disposed between the sensor package and the optical unit (see Watanbe et al., Drawing 3), the circuit board has substantially flat surfaces (see Watanbe et al., Drawing 2), the solid-state image pickup element is disposed on a surface of the sensor package (see Watanbe et

al., Drawing 3), and the seal is placed within said first opening of the circuit board (see Watanbe et al., Drawing 3). The claim differs from Watanbe et al. in that it further requires that the seal entirely covers said second opening.

In the same field of endeavor, Shinbori et al. teaches a solid-state imaging device (Figure 5) assembly having a solid-state imaging device (Figure 5, solid-state imaging device "5"). The solid-state imaging device is placed in a package having an opening (Figure 5, Figure 7). The opening is entirely covered by a glass seal plate (Figure 5, glass plate "7"; Col. 3, Lines 5-7). In light of the teaching of Shinbori et al., it would have been obvious to one of ordinary skill in the art to replace the transparence plate and transparence resin with a glass seal plate that covers the entire opening in the package of Watanbe et al., because an artisan of ordinary skill in the art would recognize that this would alleviate the use the resin and allow for protection of the imaging device (see Shinbori et al., Col. 3, Lines 5-7).

As to claim **5**, Watanbe et al. teaches a method of producing a solid-state image pickup device (see Watanbe et al., Drawings 1,2 and 3) comprising the steps of: providing a circuit board with a first opening (see Watanbe et al., Drawings 2 and 3, circuit board "22" with opening aperture "23"); joining a sensor package with a second opening (see Watanbe et al., Drawing 2 and 3, solid-state image sensor package "20"; [0016], Lines 1-6), in which a chip of a solid-state image pickup element is placed (see Watanbe et al., Drawing 1, sensor chip "11"), to one surface of the circuit board so that a light-receiving surface of the chip of the solid-state image pickup element opposes said first opening of the circuit board (see Watanbe et al., Drawing 3; Drawing 1, light-receiving side "12"); placing a seal, within said first opening of the circuit board, for sealing in the solid-state image pickup element (see Watanbe et al., Drawings 2 and 3,

transparence plate "19" in opening "23" of circuit board "22"); and disposing and joining an optical unit at and to the other surface of the circuit board so that incident light is focused on the light-receiving surface (see Watanbe et al., Drawing 3, optical unit "25"), wherein, the circuit board is disposed between the sensor package and the optical unit, the circuit board has substantially flat surfaces (see Watanbe et al., Drawing 3), and the solid-state image pickup element is disposed on a surface of the sensor package (see Watanbe et al., Drawing 1). The claim differs from Watanbe et al. in that it further requires that the seal entirely covers said second opening.

In the same field of endeavor, Shinbori et al. teaches a solid-state imaging device (Figure 5) assembly having a solid-state imaging device (Figure 5, solid-state imaging device "5"). The solid-state imaging device is placed in a package having an opening (Figure 5, Figure 7). The opening is entirely covered by a glass seal plate (Figure 5, glass plate "7"; Col. 3, Lines 5-7). In light of the teaching of Shinbori et al., it would have been obvious to one of ordinary skill in the art to replace the transparence plate and transparence resin with a glass seal plate that covers the entire opening in the package of Watanbe et al., because an artisan of ordinary skill in the art would recognize that this would alleviate the use the resin and allow for protection of the imaging device (see Shinbori et al., Col. 3, Lines 5-7).

As to claim **9**, Watanbe et al., as modified by Shinbori et al., teaches a solid-state image pickup device according to Claim 1, wherein the seal is a glass seal (see Shinbori et al., Col. 3, Line 5).

As to claims **18** and **19**, Watanbe et al., as modified by Shinbori et al., teaches a solid-state image pickup device and method of producing the same according to claims 1 and 5.

Although Watanbe does not state it explicitly, **Official Notice** is taken that the use of die bonding in connecting elements with a circuit board is well known and expected in the art. One of ordinary skill in the art would recognize that this is an effective way to provide connection in the field of semiconductors.

2. Claims 2,3,6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanbe et al. (Japanese Publication Number: H09-055487) in view of Shinbori et al. (US # 4,594,613) and further in view of Ackland et al. (Non-Patent Literature).

As to claim **2**, Watanbe et al., as modified by Shinbori et al., teaches a solid-state image pickup device of claim 1. The claim differs from Watanbe et al., as modified by Shinbori et al., in that it further requires that the sensor package include a signal processing circuit for processing a signal of the solid-state image pickup element.

In the same field of endeavor, Ackland et al. teaches a signal processing circuit on the same chip as the sensor package (see Figure 1: Conventional Multimedia camera). In light of the teaching of Ackland et al., it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the sensor Watanbe et al., as modified by Shinbori et al., to include the signal processing circuitry of Ackland et al. Such a modification would allow for all of the processing to be done on a single chip; consequently, consuming less power and minimizing the space taken up on the circuit board.

As to claim **3**, the limitations of claim 3 can be found in claim 2. Therefore, claim 3 is analyzed and rejected as previously discussed with respect to claim 2.

As to claims **6** and **7**, claims 6 and 7 are method claims corresponding to the apparatus claims 2 and 3, respectively. Therefore, claims 6 and 7 are analyzed and rejected as previously discussed with respect to claims 2 and 3, respectively.

3. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanbe (Japanese Publication Number: H09-055487) in view of Shinbori et al. (US # 4,594,613) and further in view of Tullis (US # 6,535,243).

As to claim **4**, Watanbe et al., as modified by Shinbori et al., teaches a solid-state image pickup device of claim 1. The claim differs from Watanbe et al, as modified by Shinbori et al., in that it further requires that the circuit board be connected to an external device without a connector.

In the same field of endeavor, Tullis teaches a connection between a computer and a digital camera via a wireless link (see Abstract, Lines 1-4; Figure 1; Col. 3, Lines 62-67). In light of the teaching of Tullis, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Watanbe et al., as modified by Shinbori et al., to include a wireless link to an external device. Such a modification would save space on the circuit board due to the smaller size of antennas to connectors.

As to claim **8**, claim 8 is a method claim corresponding to the apparatus claim 4. Therefore, claim 8 is analyzed and rejected as previously discussed with respect to claim 4.

Conclusion

1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony J. Daniels whose telephone number is (571) 272-7362. The examiner can normally be reached on 8:00 A.M. - 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571) 272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AD
10/26/2007

LIN YE
SUPERVISORY PATENT EXAMINER